

FIG.1 PRIOR ART

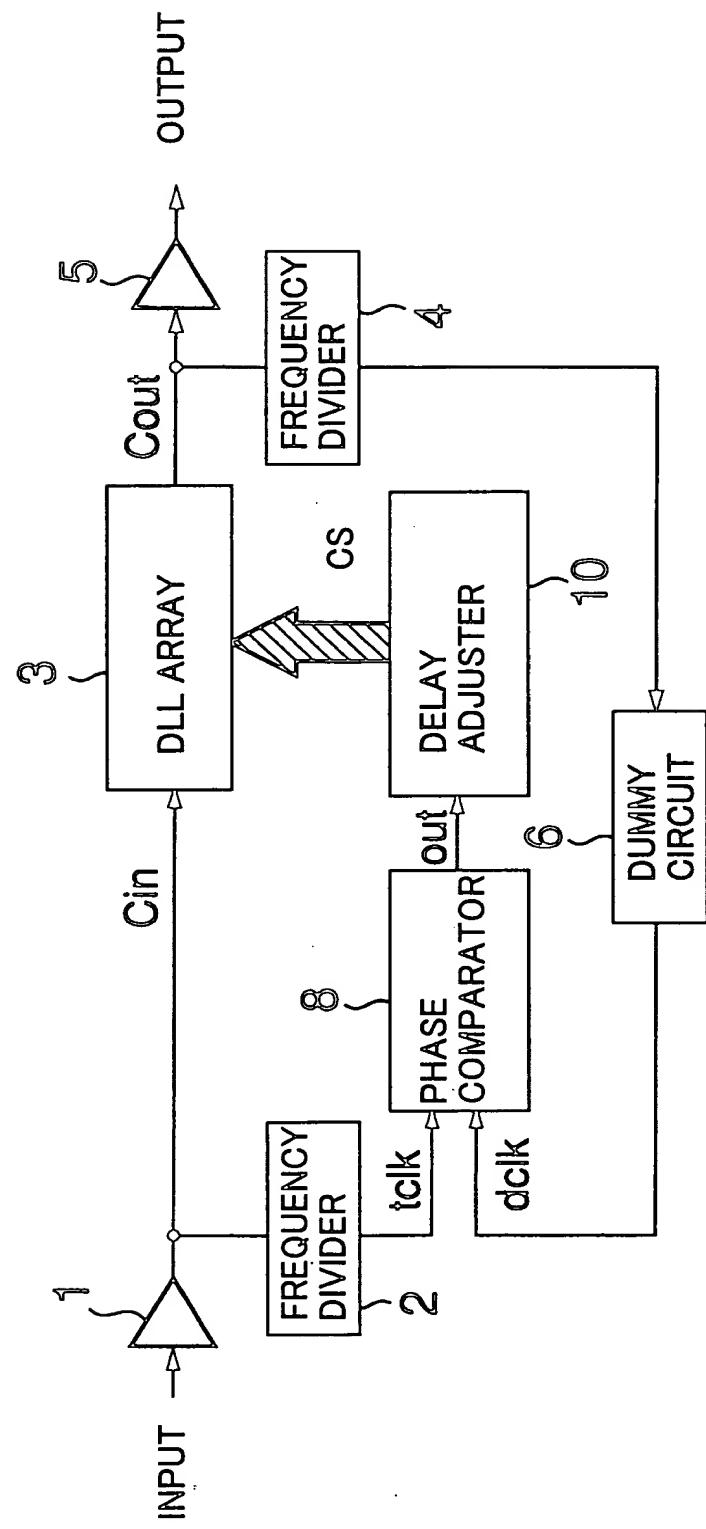
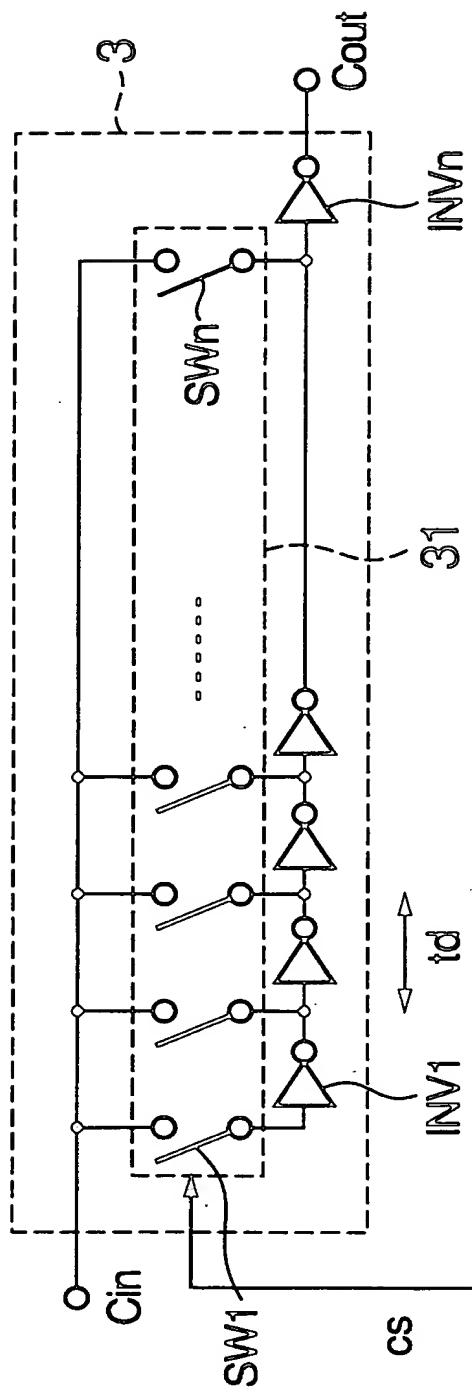
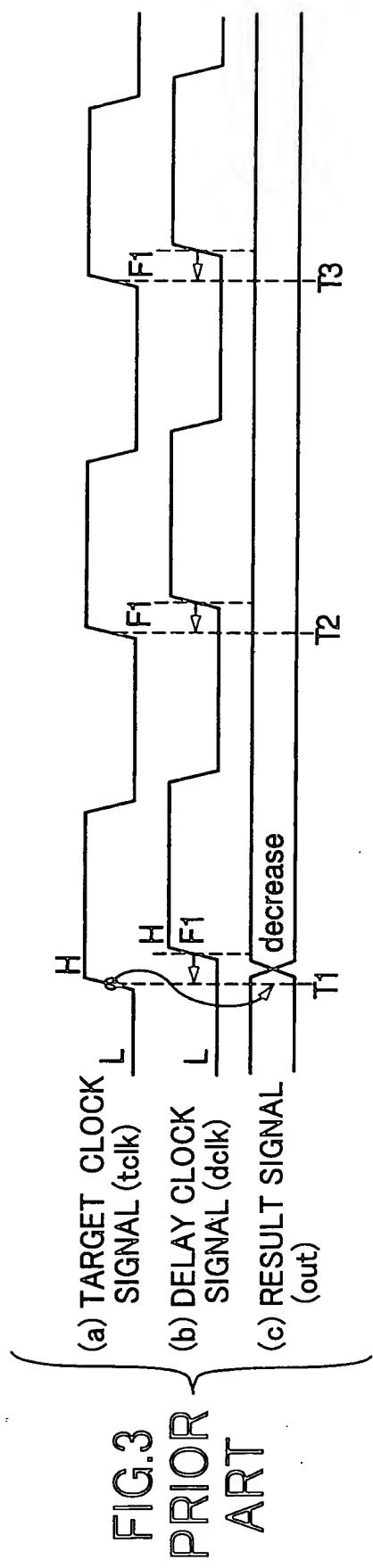
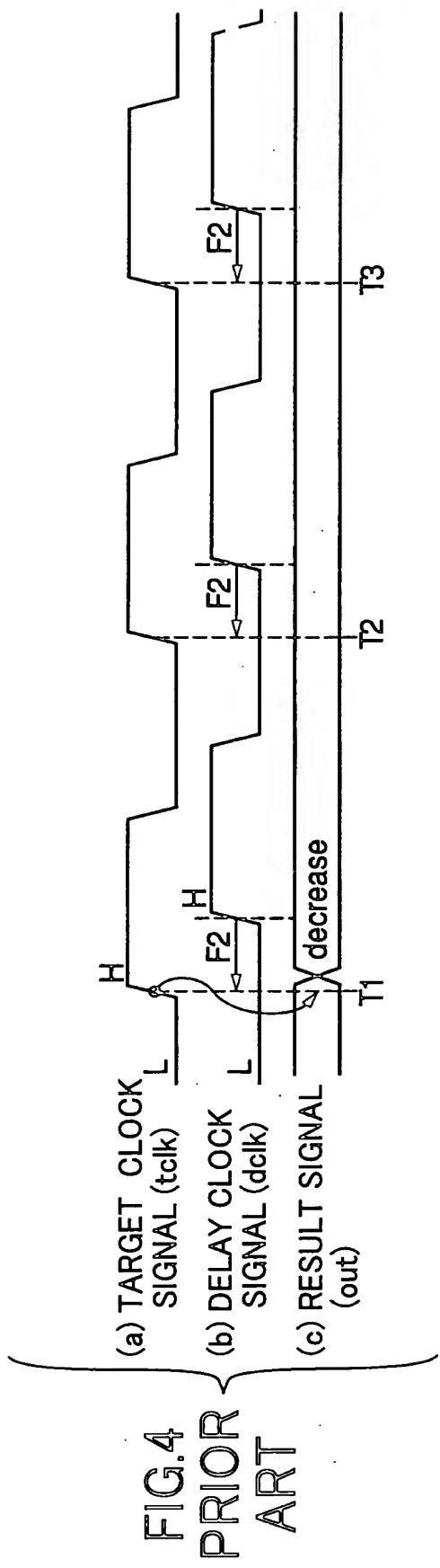
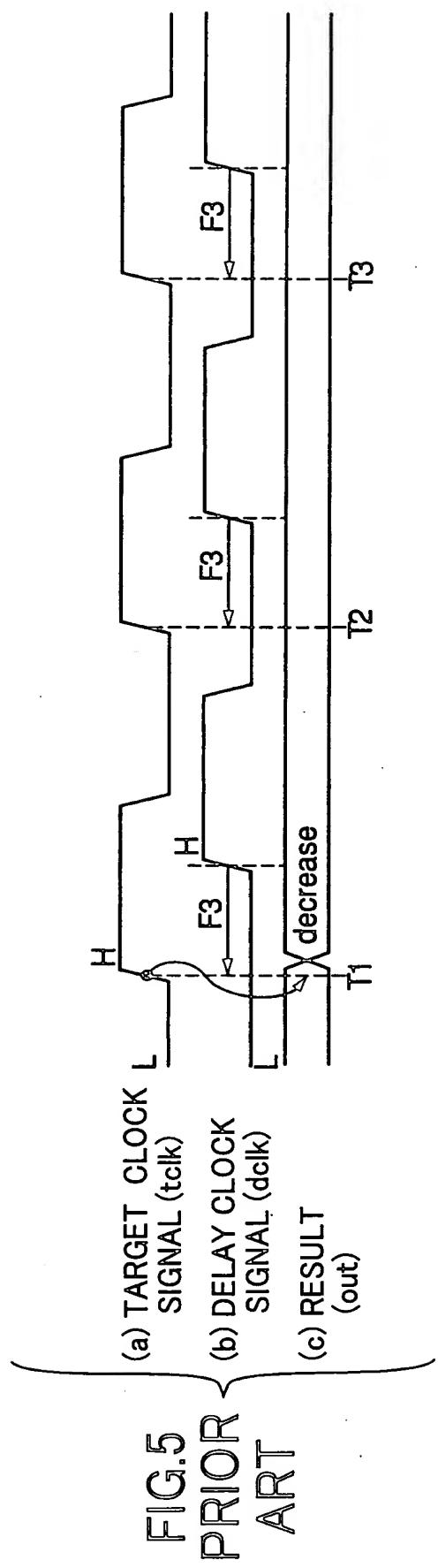


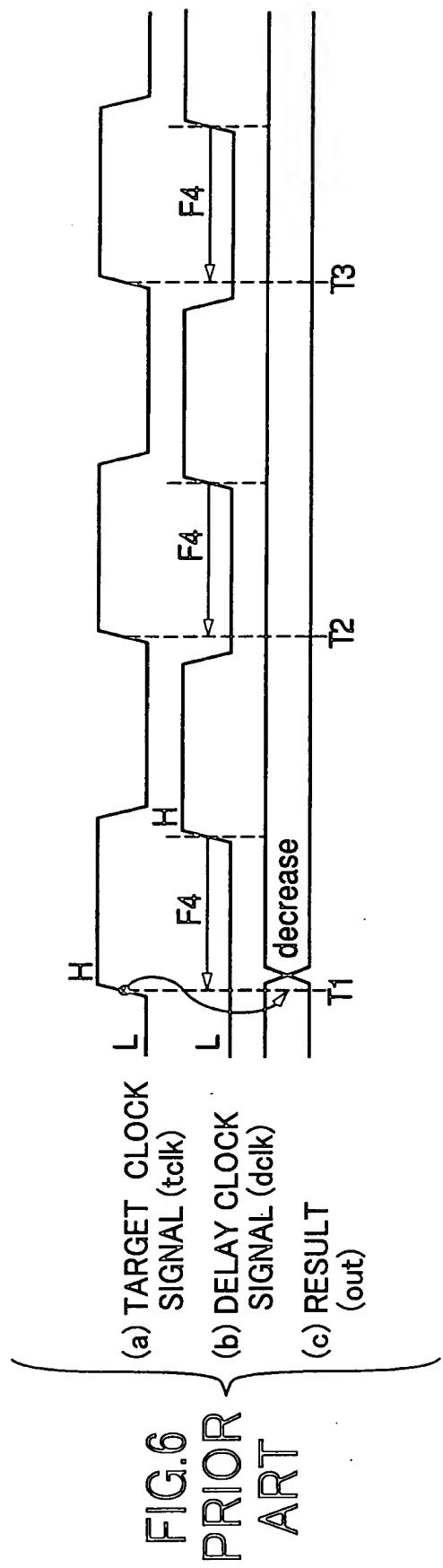
FIG.2 PRIORITY ART











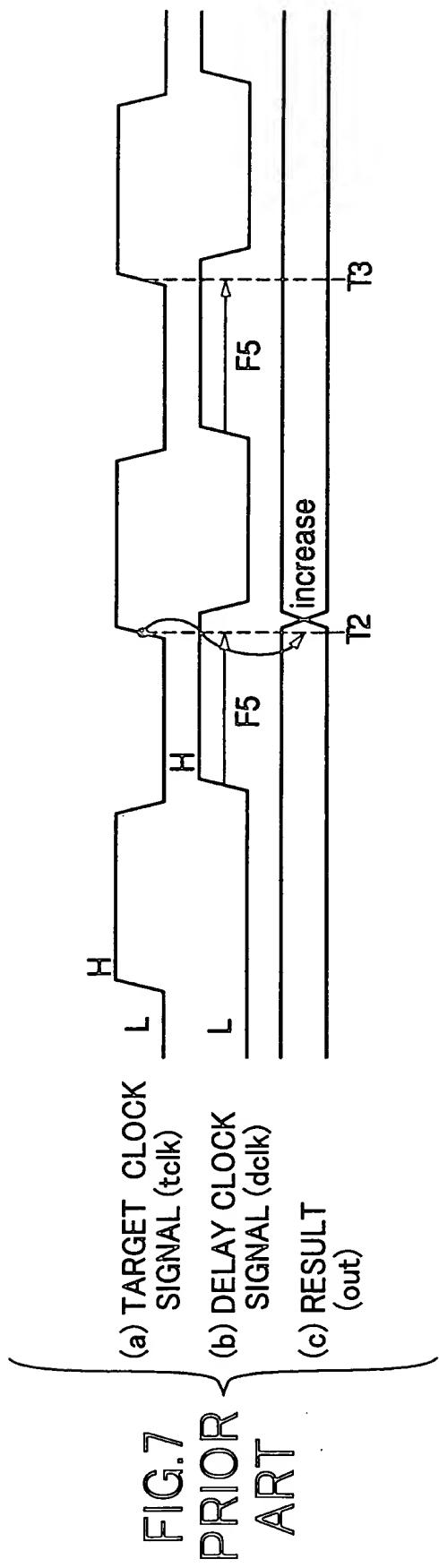
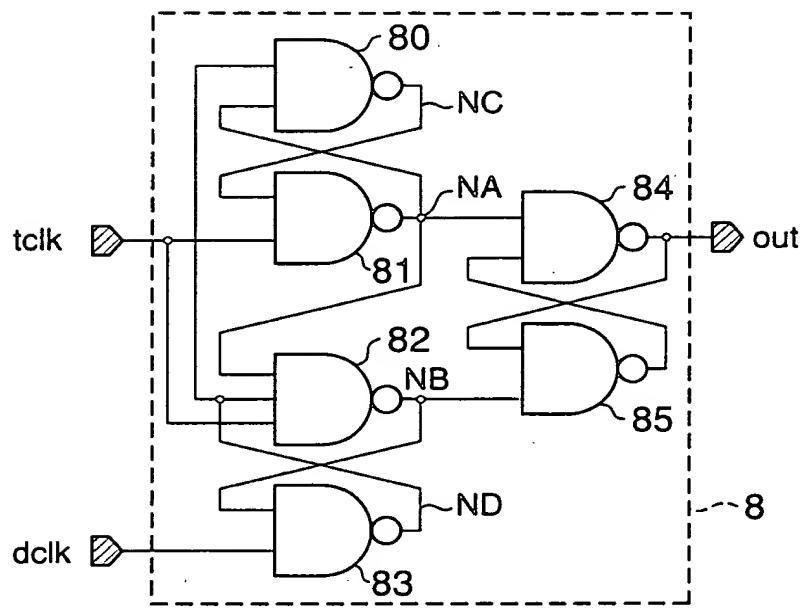


FIG. 8 PRIOR ART



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FIG. 9
PRIOR
ART

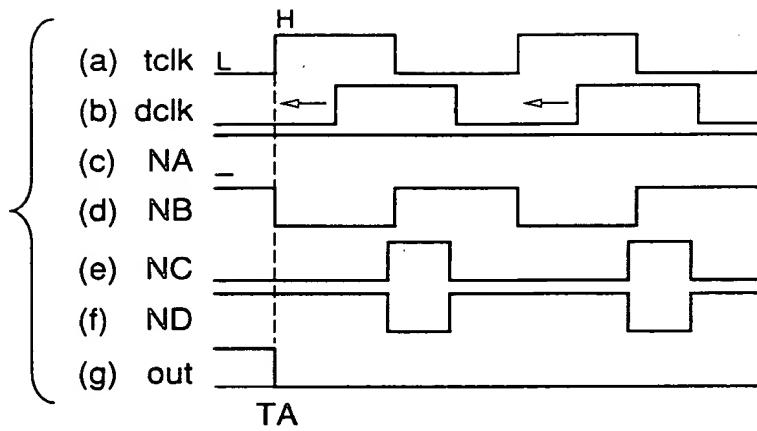


FIG. 10
PRIOR
ART

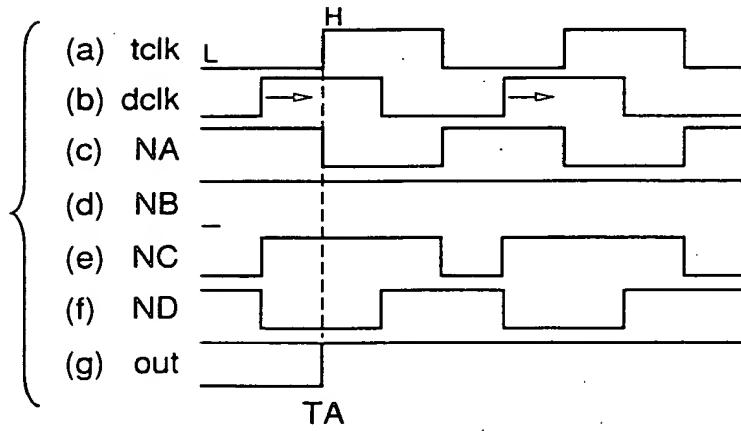


FIG. 11

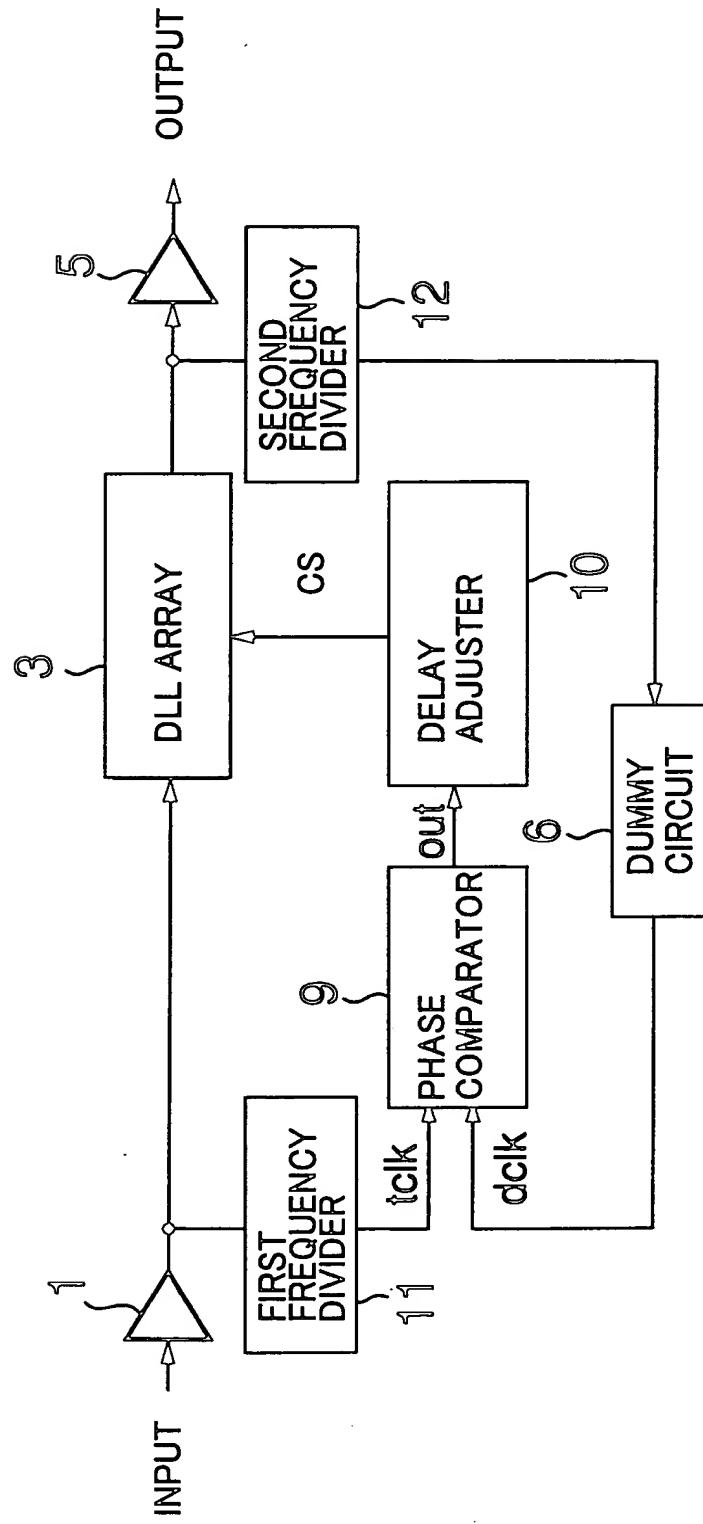
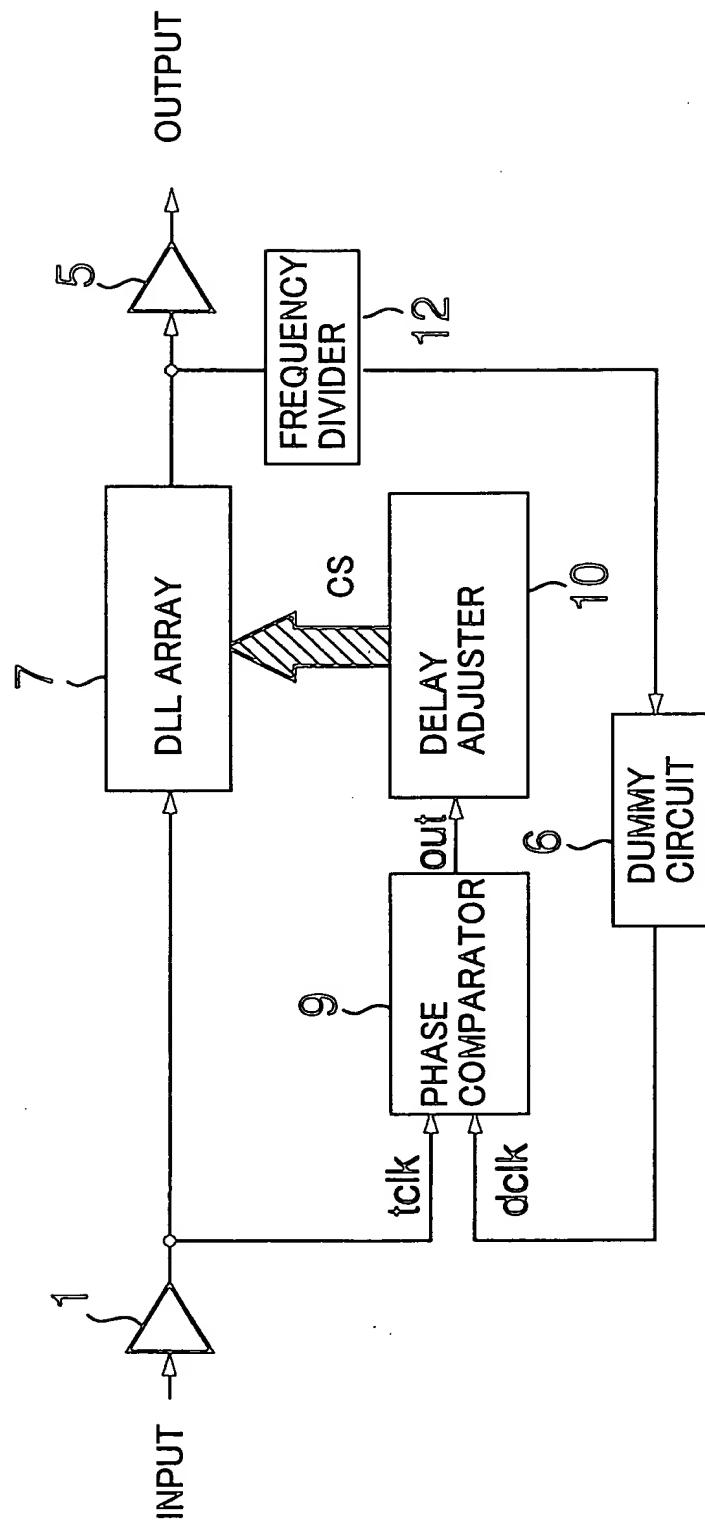


FIG. 12



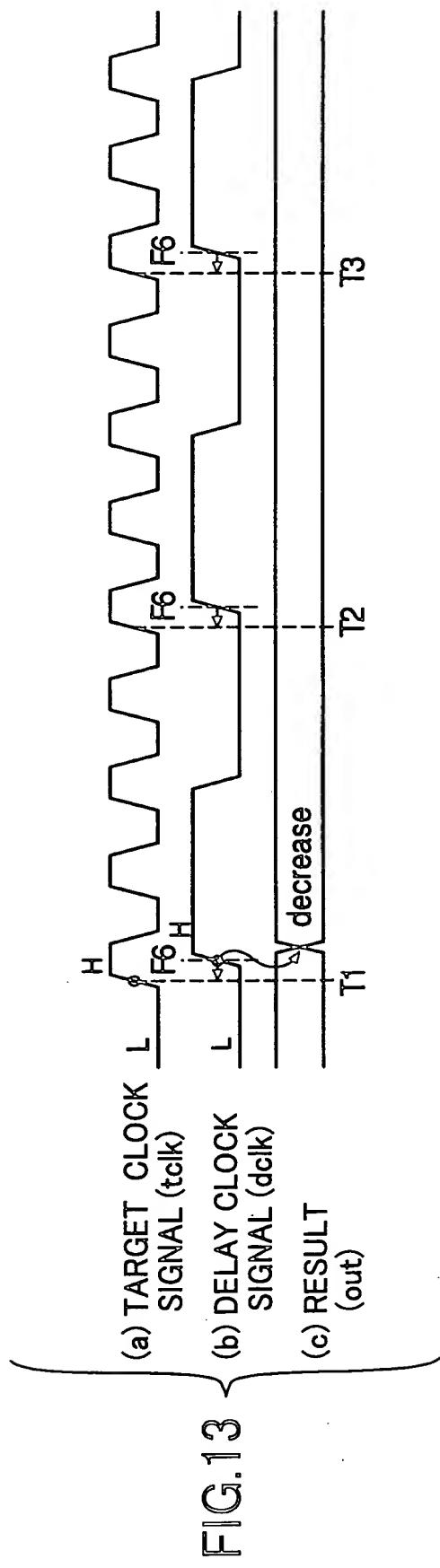
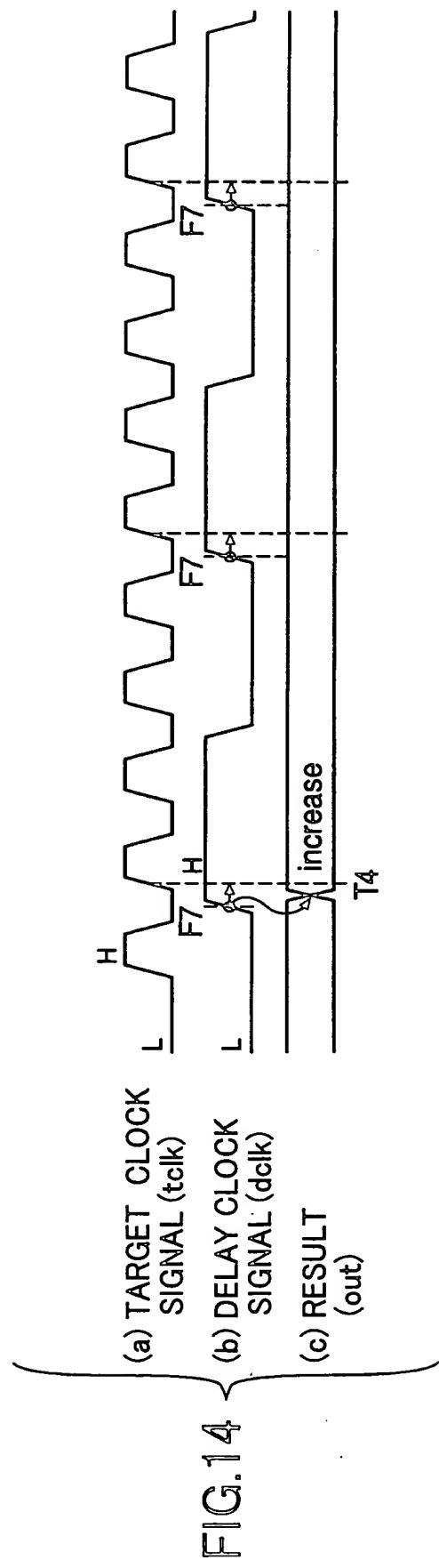
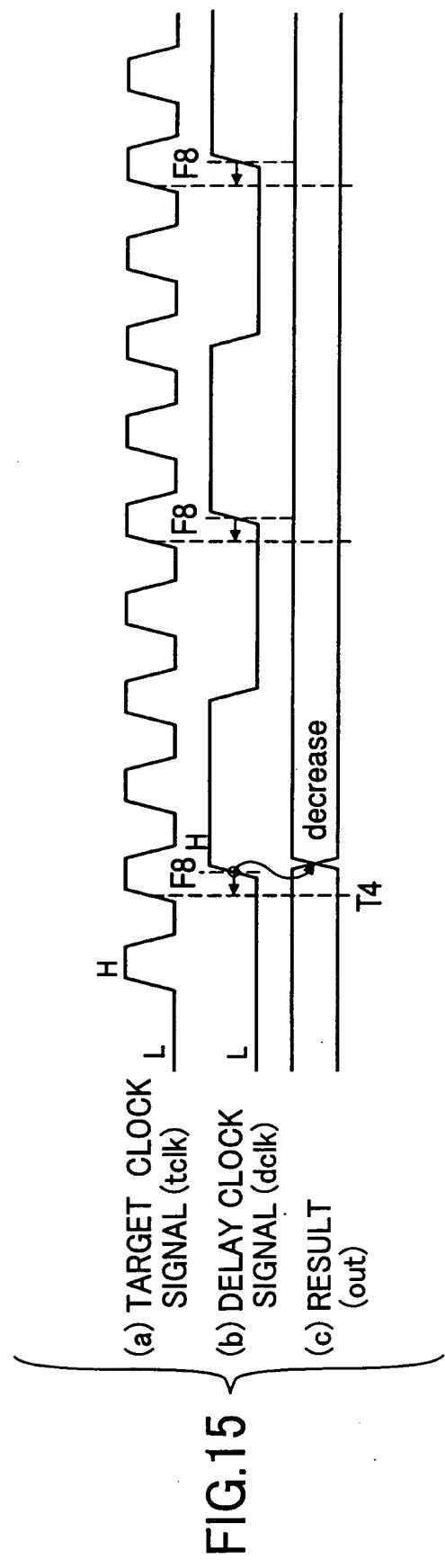
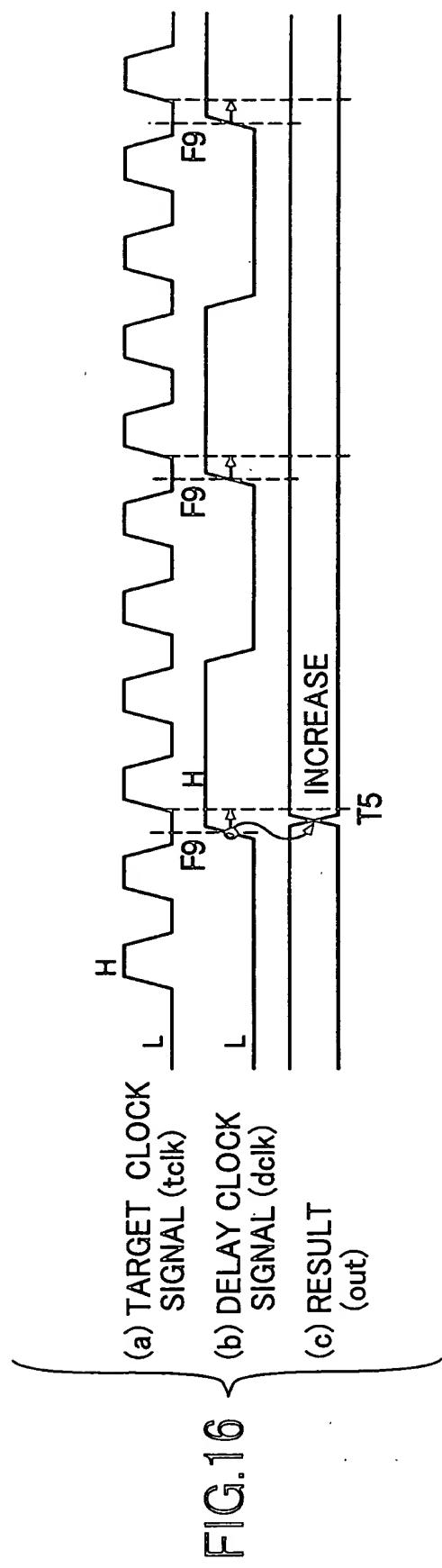


FIGURE 14: DIGITAL LOGIC







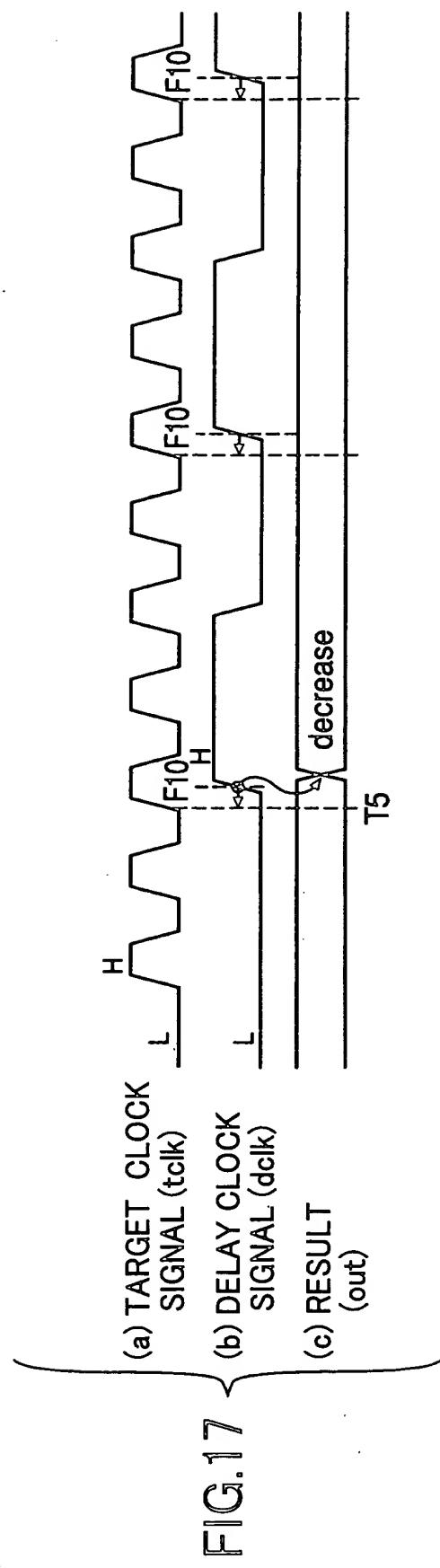


FIG. 18

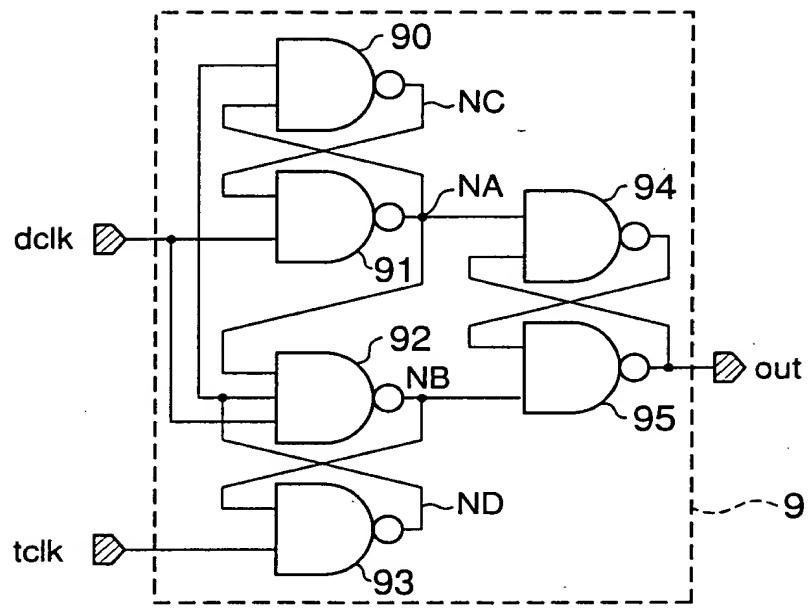


FIG. 19

